AHMED ABUHJAR
(EIT)

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Dedicated and results-driven professional with a passion for contributing to cutting-edge processor design in deep submicron technologies. Proven expertise in standard cell library design, layout composition, and spearheading transistor-level circuit design concepts. Seeking a challenging role where my skills in performance analysis processes, layout automation, and strong proficiency in scripting languages can drive innovation and excellence in semiconductor design.

Skills

SCRIPTS AND PROGRAMMING LANGUAGES
Verilog
VHDL
SystemVerilog
Python
C
MATLAB
Make

ELECTRONIC DESIGN AUTOMATION SOFTWARES (EDA) / CAD
Cadence Virtuoso
Intel Quartus Prime
EAGLE

SIMULATION AND APPLICATION SOFTWARES
ModelSim
Xilinx Vivado
ChipScope
OrCAD PSPICE

PROTOCOLS
PCIe
AXI
ACK/NACK
MOESI

OTHER SKILLS
RTL Design
Tomasulo
Computer Architecture
Semi-Custom Design
GPGPU

Education

University of Southern California - Los Angeles, California, United States — Jan. 2020 to Dec. 2021
Master of Science, Electrical Engineering - VLSI design 2021
GPA : 3.95/4.00 (MS Honors, <5% admitted)
Courses: Digital System Design (EE560), VLSI System Design (EE577a, EE577b), DFT (EE658), Asynchronous VLSI Design (EE552), Computer Systems Organization (EE457), MOS VLSI Circuit Design(EE477L), CMOS/Nano Neuromorphic Circuits (EE582), Directed Research (EE590)

Iowa State University - Ames, Iowa, United States — Aug. 2015 to May 2019
Bachelor of Science, Electrical Engineering - 3.5 years 2019

Passed Fundamentals of Engineering Exam (EIT) (Oct. 2019)

Employment

Apple Inc — 555 N Mathilda Avenue, Sunnyvale - CA
SoC Physical Design Verification Engineer — Jan. 2022 to Current
- Leveraged expertise in low-power design to conduct logic synthesis using Cadence Innovus, strategically optimizing designs for minimized power consumption while maximizing chip density.
- Collaborated seamlessly with cross-functional teams, including CAD and Technology, to successfully bring up and validate design flows, ensuring smooth project execution using cutting-edge technology.
- Strategically cooperated with package and floor-plan teams, overseeing IO pad placement and meticulous RDL routing planning to avoid signal degradation and congestion.
- Played a pivotal role by working closely with the implementation team throughout the entire chip design cycle, ultimately leading to sign-off closure for tape-out.
- Demonstrated effective leadership by successfully managing project schedules and providing crucial support to various cross-functional engineering efforts.

Apple Inc — One Apple Park Way, Cupertino - CA
SoC Physical Design Engineer (Internship) — May 2021 to Aug. 2021
- Utilized strong proficiency in scripting languages, including Python, and Make, to develop automation methods and algorithms for efficient chip design flow.
- Implemented Physical Verification automated solution project using Python script.
- Worked with team members to develop test cases and ensure project accuracy and usefulness.

USC — University of Southern California, Los Angeles - CA
Mentor for MOS VLSI Circuit Design (EE 477L) — Jan. 2021 to Dec. 2021
- Conducted laboratory discussions online via Zoom to discuss with students several techniques of CMOS design using Cadence.
- Prepared subjects, instructional materials, and answered students questions on DEN's forum as part of a team of 4 teaching assistants.

Whirlpool Corporation — 2800 220th Trail, Amana - IA
Controls Engineer (Internship) — Jan. 2017 to Jan. 2018
- Delivered cost saving and quality projects resulting in decreased production cost, lowered service incident rate and reduced failure caused by workmanship at production line.
- Built working partnerships to ensure product quality and improved performance scorecard.

Projects

Cardinal NIC and Chip Multiprocessor — Jan. 2021 to May 2021
- Developed a complete network interface component, routers, cardinal processors and arbitration logic using Verilog and simulated a real-world RTL2GDS flow.
- Conducted synthesis using Cadence Innovus to optimize logic, resulting in improving power consumption and performance.
- Utilized Innovus for power and clock distribution, ensuring robust power delivery and clock synchronization.
- Conducted place and route techniques to minimize wire length and maximize chip density.
- Performed equivalence checking processes to ensure functional consistency between RTL and gate-level designs.
- Successfully achieved timing closure, resolving critical path issues and meeting design objectives and timing constraints.

CNN with Asynchronous NoC — Jan. 2021 to May 2021
- Implemented Convolutional Neural Network (CNN) and Network on Chip (NoC) in an asynchronous design style using System Verilog.
- Designed Micro-architectural blocks including Routers, Processing Elements and Memories.
- Verified correctness of operation for each block by running simulations using identified test cases in a test-bench.

VLSI CMOS Design - 1024bit Low Power SRAM — Aug. 2020 to Dec. 2020
- Designed 10-T SRAM cells with noise margins as criteria using Cadence Virtuoso.
- Implemented three low-power techniques including clock gating to minimize the dynamic and leakage power consumption.
- Performed thorough power and noise analysis to enhance power efficiency and signal integrity.
- Implemented Python code to generate vector files used to simulate and test the design with several input stimulus.

Tomasulo-based processor system implemented in VHDL — May 2020 to July 2020
- Designed Re-Order Buffer in VHDL to achieve in-order commitment and to support exceptions.
- Implemented Register-Renaming using Register Aliasing Table to solve WAW and WAR hazards.
- Fulfilled branch prediction and speculative execution beyond branch with help of Branch Prediction Buffer and Return Address Stack.
- Achieved Copy-Free-Checkpointing to restore pipeline status upon branch mis-predictions.
- Simulated design using ModelSim, synthesized on FPGA, tested for numerous instruction streams and debugged with help of ChipScope.

Physical Layer Design (Tx and Rx) of PCIe protocol — May 2020 to July 2020
- Implemented clock gating, 8b/10b Decoder and Encoder, Elastic Buffer, Deskew Buffer in Verilog.
- Integrated, simulated and synthesized the complete design using Xilinx Vivado and debugged using ChipScope.