

AHMED ABUHJAR

(EIT)

✉ abuhjar@usc.edu
🌐 www.aabuhjar.com
☎ +1 (714) 653-0714
📍 Los Angeles
in ahmed-abuhjar

Electrical engineering student possessing excellent skills in Digital VLSI Design and Computer Architecture. Seeking full-time or internship opportunities to provide elegant solutions by utilizing developed design and verification skills.

Skills

SCRIPTS AND PROGRAMMING LANGUAGES

Verilog
VHDL
SystemVerilog
Python
C
MATLAB
C++
Java

ELECTRONIC DESIGN AUTOMATION SOFTWARES (EDA) / CAD

Cadence Virtuoso
Intel Quartus Prime
EAGLE

SIMULATION AND APPLICATION SOFTWARES

ModelSim
Xilinx Vivado
ChipScope
OrCAD PSPICE

PROTOCOLS

PCIe
AXI
ACK/NACK
MOESI

OTHER SKILLS

RTL Design
Tomasulo
Computer Architecture
Semi-Custom Design
GPGPU

Education

University of Southern California

Master of Science, Electrical Engineering - VLSI design | Dec 2021
GPA : 3.95/4.00
Courses: Digital System Design (EE560), VLSI System Design (EE577a, EE577b), DFT (EE658), Asynchronous VLSI Design (EE552), Computer Systems Organization (EE457), MOS VLSI Circuit Design (EE477L), CMOS/Nano Neuromorphic Circuits (EE582), Directed Research (EE590)

Iowa State University

Bachelor of Science, Electrical Engineering - 3.5 years | May 2019

Passed Fundamentals of Engineering Exam (EIT) (Oct. 2019)

Projects

CNN with Asynchronous NoC

January 2021 - May 2021

- Implemented Convolutional Neural Network (CNN) and Network on Chip (NoC) in an asynchronous design style using System Verilog.
- Designed Micro-architectural blocks including Routers, Processing Elements and Memories.
- Verified correctness of operation for each block by running simulations using identified test cases in a test-bench.

VLSI CMOS Design - 1024bit Low Power SRAM

August 2020 - December 2020

- Designed 10-T SRAM cells with noise margins as criteria using Cadence Virtuoso.
- Implemented three low-power techniques including clock gating to minimize the dynamic and leakage power consumption.
- Implemented Python code to generate vector files used to simulate and test the design with several input stimulus.

Physical Layer Design (Tx and Rx) of PCIe protocol

May 2020 - July 2020

- Implemented clock gating, 8b/10b Decoder and Encoder, Elastic Buffer, Deskew Buffer in Verilog.
- Integrated, simulated and synthesized the complete design using Xilinx Vivado and debugged using ChipScope.

IoT Environmental Monitoring System

August 2018 - May 2019

- Designed a low-cost hygroscopic soil moisture sensor to detect change in moisture level.
- Designed low-cost custom PCBs for sensor nodes to receive and transmit signals between each other and the network gateway.
- Tested sensors under various environmental conditions to calibrate and determine moisture level range in which the sensors operate as linear devices.
- Exchanged project ideas with team members to assure building a strong sense of reciprocity.

VLSI Semi-Custom CMOS Design - Temperature Sensor Using Diodes

January 2018 - May 2018

- Utilized Cadence and ModelSim to design circuits including PTAT, ADC, and 7-segment display.
- Implemented Python code to generate vector files to simulate and test the design and to improve its accuracy of measurements to 2 degrees Celsius.
- Performed DRC and LVS tests on layouts to ensure all circuits meet fabrication rules and match schematics before fabrication.

Experience

USC - Mentor for MOS VLSI Circuit Design (EE 477L) - Los Angeles, California

January 2021 - May 2021

- Conducted laboratory discussions online via Zoom to discuss with students several techniques of CMOS design using Cadence.
- Prepared subjects, instructional materials, and answered students questions on DEN's forum as part of a team of 4 teaching assistants.

Whirlpool Corporation - Controls Engineer Internship - Middle Amana, Iowa

June 2017 - January 2018

- Delivered cost saving and quality projects resulting in decreased production cost, lowered service incident rate SIR and reduced failure caused by workmanship at production line.
- Built working partnerships to ensure product quality and improved performance scorecard.

Iowa State University - C Teaching Assistant - Ames, Iowa

January 2017 - May 2017

- Organized practical C programming supplemental lectures and tutored students to help understand programming and develop problem solving and debugging techniques.